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PATENT
Atty. Ref. No. 1011-57087

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Suaya & Gabillet

Art Unit: 2858

Application No.: 09/385,666

Filed: August 26, 1999

For: CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT

Examiner: Phan, Thai Q.

Date: February 10, 2003

CERTIFICATE OF MAILING
I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service on February 10, 2003, as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Attorney for Applicant

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

AMENDMENT

Responsive to the Office action dated November 20, 2002, please amend the subject application as follows:

In the Drawings:

A Request for Approval of Drawing Corrections showing corrections to Figs. 1-6 and 8-10 in red ink is filed concurrently herewith. Applicants request approval of the indicated corrections. If the drawing corrections are approved, Applicants request that the enclosed corrected formal drawings, renumbered 1-9, be substituted.

In the Specification:

Please replace the paragraph beginning at page 5, line 18 with the following paragraph:

B1 Figure 7 is a block diagram illustrating an overview of an IC design simulation tool.

Please replace the paragraph beginning at page 6, line 1 with the following paragraph:

B2 Figure 8 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention.